REMARKS/ARGUMENTS

The final office action of May 16, 2007, has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. This response is being filed concurrent with the filing of a Request for Continued Examination. Claims 1, 10, and 12 have been amended to place the claims in a more preferred form. Claims 9 and 11 has been canceled without prejudice or disclaimer. Claims 1-8, 10, and 12-25 remain in this application.

Claims 1-6, 9-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,760,277 B1 to Farooq ("*Farooq*") in view of U.S. Patent No. 6,996,758 B1 to Herron, et al. ("*Herron*"). Claims 7 – 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Farooq* and *Herron* as applied to Claim 6, and in further view of U.S. Patent No. 6,621,767 B1 to Kattan ("*Kattan*"). Applicants respectfully traverse these rejections.

Applicants' amended claim 1 recites, among other features,

> configuring each configurable logic block of the second set to respond with a deterministic output to an *N*-bit input,
>
> wherein the configuring the first set includes configuring a configurable logic block of the first set as a verifier to verify a responsive output of the second set organized into *M* groups of configurable logic blocks,
>
> wherein the verifier is configured to accept its own output as one bit of the *N*-bit input,
>
> wherein, upon the output of the verifier being a failure indicator, the verifier is configured to maintain the failure indicator for the test.

The combination of *Farooq* and *Herron*, even if proper, fails to teach or suggest at least these features of Applicants' amended claim 1. Neither *Farooq* or *Herron*, alone or in combination, teach or suggest a verifier, configured to accept its own output as one bit of the N-bit input and to maintain a failure indicator for the remainder of the test when a failure occurs. As such, because *Farooq* and *Herron*, either alone or in combination, fail to teach or suggest each and every feature of Applicants' claim 1, withdrawal of the rejection is respectfully requested.

Applicants' claims 2-12, which depend on claim 1, are patentably distinct over the art of record for at least the same reasons as their ultimate base claim and further in view of the novel features recited therein. For example, Applicants' claim 3 recites, among other features,

"configuring a third set of configurable logic blocks to be second testing circuitry; and operating the third set, concurrently with the first set, to test a fourth set of configurable logic blocks." The combination of *Farooq* and *Herron*, even if proper, fails to teach or suggest at least this feature. In particular, the combination of references fails to teach concurrent operation of sets to test another set.

Claims 13-17 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,036,473 to Butts, et al. ("*Butts*") in view of U.S. Patent No. 6,470,485 B1 to Cote, et al. ("*Cote*"). Applicants respectfully traverse this rejection.

Even assuming, without admitting, that the combination of *Butts* and *Cote* is proper, the combination fails to teach or suggest each and every feature of Applicants' claim 13. Applicants, as in their previous responses, still contend that *Butts* fails to teach the features in claim 13, which recites among other features, "configuring a second routing portion to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second configuration inverse to the first configuration." The Action cites col. 2 lines 15-19 of *Butts* for support, alleging that *Butts* describes this feature, "An 'interconnect chip' is an electronically reconfigurable device which can implement arbitrary interconnections among its I/O pins. A 'routing chip' is an interconnect chip used in a direct or channel routing interconnect." The Action alleges that "[i]mplementing arbitrary interconnections among the I/O pins comprise inverse configuration." Applicants respectfully disagree.

On the contrary, "arbitrary interconnections among I/O pins" by no means implies or suggests an "inverse configuration." The fact that *Butts* describes a reconfigurable device that can implement arbitrary interconnections among its I/O pins does not imply a second configuration inverse to the first configuration. Applicants, therefore, still contend that *Butts* fails to teach or suggest, "configuring a second routing portion to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second configuration inverse to the first configuration." As such, because the combination of *Butts* and *Cote* fails to teach or suggest each and every feature of Applicants' claim 13, withdrawal of the rejection is respectfully requested.

Applicants' claims 14-17, which depend on claim 13, are patentably distinct over the art of record for at least the same reasons as their ultimate base claim and further in view of the novel features recited therein.

Applicants' claim 23 includes similar features as described above with reference to claim 13. As such, Applicants' claim 23 is patentably distinct over the art of record for at least similar reasons as described with respect to claim 13.

Claim 18-20 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Cote* in view of U.S. Patent No. 6,874,107 to Lesea ("*Lesea*"). Applicants respectfully traverse this rejection.

Even assuming, without admitting, that the combination of *Cote* and *Lesea* is proper, the combination still fails to teach or suggest each and every feature of Applicants' claim 18. Applicants' claim 18 recites, among other features, "wherein the first set is configured to provide a second test pattern to test the second set, and the second set is configured to output data in response to the second test pattern received from the first set." The cited portion of *Lesea* states that "[i]n another embodiment, a field programmable gate array (FPGA) comprises input and output data communication connections, a serializer/deserializer circuit coupled to the output data connection. The logic array is further programmed to check a data pattern received on the input connection while performing a built in self test operation. After test, the circuit may be re-programmed as stated above." While *Lesea* may describe a field programmable gate array (FPGA) that comprises input and output data communication connections, a serializer/deserializer circuit coupled to the output data connection, *Lesea* does not describe the above noted feature of Applicants' claim 18. In particular, *Lesea* does not explicitly describe a second test pattern to test the second set, and the second set is configured to output data in response to the second test pattern received from the first set.

Furthermore, Applicants' claim 18 recites, among other features, "wherein the first set is further configured to provide an *N*-bit input generator to the second set and to provide a configurable logic block, separate from the *N*-bit input generator, as a verifier to verify the output data of the second set." Per the cited portion of *Lesea* above, *Lesea* describes a logic array that performs a built-in self test operation. Notably, the logic array performs the test operation

within itself, not separately. Therefore, *Lesea* clearly fails to describe the above noted feature of Applicants' claim 18. In particular, *Lesea* fails to explicitly describe a configurable logic block, separate from the *N*-bit input generator, as a verifier to verify the output data of the second set.

Cote fails to teach or suggest the above features of Applicants' claim 18 as well. As such, the combination of references fails to teach or suggest each and every feature of Applicants' claim 18 and withdrawal of the rejection is respectfully requested.

Claims 19-20, 22, which depend from claim 18, are allowable over the art of record for all the reasons given above concerning their respective base claim, and further in view of the novel features recited therein.

Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,903,744 to Tseung, et al. ("*Tseung*") in view of *Cote*. Applicants respectfully traverse this rejection.

Even assuming, without admitting, that the combination of *Tseung* and *Cote* is proper, the combination fails to teach or suggest each and every feature of Applicants' claim 24. Applicants, as in their previous responses, still contend that *Cote* fails to teach the feature in claim 24, which recites, among other features, "wherein the data processing portion is configured to provide a first test pattern to the first set to test the second set and a second test pattern to the second set to test the first set." As admitted by the Action, *Tseung* fails to teach such a feature. In rejecting this feature, the Action relies on various portions of *Cote*. However, no portion of *Cote* teaches or suggests such a feature. *Cote* merely describes an implementation of FPGAs with variable gain blocks (VGB) including registers for storing current state bits (Col. 25, lines 6-26). Another cited portion of *Cote* describes a provision "[w]ithin the contemplation of the invention to provide within computer-readable media (e.g., floppy diskettes, CD-ROM, DVD-ROM) and/or within manufactured and transmitted signals, FPGA-configuring bit streams in accordance with the above disclosure and/or to provide computer-understandable instructions to computers for causing the computers to perform automated stepping of FPGA's under-test through a battery of reconfigurations and test loops and readouts in accordance with the above disclosure." (Col. 27, lines 52-61). Nothing in these descriptions suggests or teaches Applicants' claim 24 features noted above. In fact, *Cote* still describes a system that would utilize a test

pattern to self-test and not to test a different set. (Col. 27, lines 18-21). As such, the combination of *Tseung* and *Cote* fails to teach or suggest each and every feature of Applicants' claim 24 and withdrawal of the present rejection is respectfully requested.

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tseung* in view of *Butts* and *Cote*. Applicants respectfully traverse this rejection.

As stated in Applicants previous responses, the combination of references, even if proper, fails to teach or suggest each and every feature of claim 25. In particular, Applicants still contend as in their previous response, that none of the references teaches or suggests the claim 25 feature of, "wherein the second routing portion is configured to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second manner inverse to the first manner." Therefore, for at least these reasons, withdrawal of the rejection of amended claim 25 is respectfully requested. The Action asserts that *Butts* teaches this feature per col. 2 lines 15-19, which reads that "An 'interconnect chip' is an electronically reconfigurable device which can implement arbitrary interconnections among its I/O pins. A 'routing chip' is an interconnect chip used in a direct or channel routing interconnect." The Action alleges that "[i]mplementing arbitrary interconnections among the I/O pins comprise inverse configuration." Applicants respectfully disagree.

On the contrary, "arbitrary interconnections among I/O pins" by no means implies or suggests an "inverse configuration." The fact that *Butts* describes a reconfigurable device that can implement arbitrary interconnections among its I/O pins does not imply a second configuration inverse to the first configuration. Applicants, therefore, still contend that *Butts* fails to teach or suggest "configuring a second routing portion to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second configuration inverse to the first configuration." As such, because the combination of *Tseung*, *Butts,* and *Cote* fails to teach or suggest each and every feature of Applicants' claim 25, withdrawal of the rejection is respectfully requested.

CONCLUSION

All rejections having been addressed, Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same. However, if for any reason the Examiner believes the application is not in condition for allowance or there are any questions, the examiner is requested to contact the undersigned at (202) 824-3155.

Respectfully submitted,
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